Verification of Device Model by Measuring Capacitance and Static Characteristics for Predicting Switching Waveform

Kengo Koki, Masahiko Yoshioka, Kazuhiro Umetani and Eiji Hiraki
Graduate School of Natural Science and Technology
Okayama University
Okayama, Japan

Published in: 2019 IEEE International Conference on Renewable Energy Research and Application (ICRERA)

© 2019 IEEE. Personal use of this material is permitted. Permission from IEEE must be obtained for all other uses, in any current or future media, including reprinting/republishing this material for advertising or promotional purposes, creating new collective works, for resale or redistribution to servers or lists, or reuse of any copyrighted component of this work in other works.

DOI: 10.1109/ICRERA47325.2019.8996508
Verification of Device Model by Measuring Capacitance and Static Characteristics for Predicting Switching Waveform

Kengo Koki, Masahiko Yoshioka, Kazuhiro Umetani and Eiji Hiraki
Graduate School of Natural Science and Technology
Okayama University
Okayama, Japan
p69w820c@s.okayama-u.ac.jp

Abstract—Recently, as the miniaturization and densification of the power conversion circuit, switching frequency has been increased. To accomplish the densification, it is essential to predict the losses that occur in each part for the optimization of electric components. However, switching loss which needs to consider nonlinear characteristics are difficult to predict. As a solution, considering the dependence of the gate-drain capacitance on gate-source voltage may improve the prediction accuracy of switching loss. The purpose of this study is to evaluate the improvement of prediction accuracy by considering it. First, to construct the simulation model, the wiring parameter in the circuit, static characteristics and the parasitic capacitance of the device was measured. Next, the device model provided by the manufacturer to use in the simulation was adjusted. Also, the characteristics of the gate-drain capacitance on the gate-source voltage were obtained from two types of measurement circuits. As a result, it was verified that the difference which occurred at the rise of the drain-source voltage at the turn-off tends to decrease and prediction accuracy of the turn-off loss was improved by considering the characteristics of the gate-drain capacitance on the gate-source voltage. Therefore, we concluded that this consideration has the ability to the improvement of turn-off waveforms.

Keywords—switching; Spice simulation; gate-drain capacitance; wiring parameter; parasitic inductance

I. INTRODUCTION

Power conversion circuits are used in many applications, such as machinery and tools, electric vehicle (EV) [1], home appliances, digital equipment. In particular, switching devices included in power conversion circuits have mainly used Si-MOSFET. However, its performance is getting to the limit [2]. Therefore, SiC-MOSFET and GaN-FET, known as high speed switching devices have been used as the next-generation switching devices [3-5].

This attractive feature helps that power conversion circuit can be miniaturization and densification. Because of the miniaturization and the densification, to reduce the size of the components is also necessary. However, to achieve sufficient heat dissipation, we need to attach a bulky heat sink, which prevents miniaturization of components. Also, high switching frequency reduces the size of the magnetic components. However, as the switching frequency is high, heat dissipation performance is low. Hence, switching frequency and heat dissipation design performance is a trade-off relationship. Therefore, to make optimal heat dissipation design, device losses must be correctly predicted.

However, the measurement of switching waveform is becoming difficult for recent high speed switching loss devices. There are mainly three reasons. First is the frequency limit of probes. Second is the installation space of probes. Third is the signal delay of probes. For these reasons, the measurement of next-generation devices is almost impossible. Therefore, switching loss estimation by simulation is an important design tool for recent high speed switching devices.

However, there are two main problems to solve, especially in fast switching. The first problem is that there is a deviation from the device model and the actual device. The second problem is the modeling of PCB.

To solve the first problem, many studies have been reported that modeled switching device and verified prediction accuracy of switching characteristics [6-11]. According to [6], a simulation model was constructed based on information of the datasheet, and switching waveforms were compared. However, there was a deviation in the mirror period and a deviation occurs at the rise of drain-source voltage $V_{ds}$ waveform (Fig.9 conventional). In this period, gate-source voltage $V_{gs}$ is not 0V. Also, gate current flows through $C_{gd}$ and it is charged and discharged. Here, the datasheet shows the parasitic capacitance when $V_{gs}$ is 0V, but only a part of the actual power conversion circuit can be covered. Therefore, it was suggested that further modeling of $C_{gd}$ was necessary. On the other hand, the $V_{gs}$ characteristics of $C_{gd}$ was modeled in [10]. It was reported that this modeling further improved prediction accuracy. However, the characteristic of $C_{gd}$ was extracted by back calculating the switching waveform with a long mirror period. Although the modeling of the MOSFET, which was their purpose, was achieved, it does not follow our purpose of predicting the switching waveform.

Next, in PCB modeling at high speed switching, the voltage drop of the wiring parameter, especially parasitic inductance, is a significant problem [12-14]. Conventionally, the estimated value of inductance was obtained by fitting from the measured
switching waveform. However, the value of inductance is approximately a few nanohenries order and it is not practical because accurate measurement becomes increasingly difficult. To solve this problem, previous research [15,16] proposed a common source inductance (Ls) measurement method that was particularly difficult to measure in the state of being mounted on PCB and enabled to measure it. Therefore, the modeling of PCB could be done without using estimate value.

The purpose of this paper is to verify the improvement of prediction accuracy by considering the dependence of Cgd on Vgs in the model. In order to evaluate the prediction accuracy of the switching waveforms, we measured the wiring parameter in the PCB, the parasitic capacitance, and the static characteristics of the MOSFET. In this paper, we adopted the double pulse test (DPT). Also, in order to verify the accuracy of the predictions with and without consideration of the dependence of Cgd on Vgs.

The following discussion consists of 4 sections. Section II explains the construction method of the conventional model. Next, section III explains the construction method of the proposed model. Then, in section IV, the experimental result and each model are compared. Finally, section V gives the conclusions.

II. CONVENTIONAL MODEL

This section explains the conventional model. Firstly, the static characteristics and the characteristics of the parasitic capacitance to the drain-source voltage Vds of the devices shown in Table I were measured by curve tracer. Also, the parasitic inductances in the circuit (Lg, Ld, and Ls) were measured by method in [17], and parasitic resistance of main circuit loop Rd was measured by impedance analyzer.

A. Modeling of PCB

In this subsection, we measured the wiring parameter in the PCB. Also, the wiring parameter is a constant value, so measurement is very important. In order to measure the wiring parameter, we used three types of circuits.

Measurement of Ls was adopted a recently proposed method [15,16]. The measurement circuit is shown in Fig.1(a). First, another PCB with the same pattern as the experimental circuit prepared and low-side MOSFET mounted. Next, a resistor Rmesu with high impedance was mounted on the position of the gate resistance Rg. Also, a ceramic capacitor Cmesu with much larger of the gate-source capacitance in MOSFET was mounted to connect the pads for the output terminal and the ground terminal of the gate driver. In addition, we made the solder bridges to connect the pad for high-side parasitic diode. Then we applied the DC voltage to Cmesu in order to keep the MOSFET at the on-state. Finally, we connected a signal generator between the drain and source of MOSFET to supply the high-frequency sinuosoidal current and measured the AC voltage across Rmesu and AC current from the signal generator. The RMS of Vds and Vgs are defined as Vmesu and Imesu, respectively.

In the high-frequency region, Cmesu, Ciss, and Lg can regard as short because its impedance is far lower than Rmesu. Therefore, Vmesu, the voltage drops at Rmesu and L on are approximately the same. Consequently, the value of Ls can be calculated as

\[ L_s = \frac{V_{\text{mesu}}}{2\pi f_{\text{ac}}} \sin \phi, \]

where \( f \) is the frequency of AC current and \( \phi \) is the phase difference between the voltage drop at Rmesu and the AC current \( i_{\text{ac}} \).

In this paper, we measured at nine AC frequency from 2MHz to 10MHz. Also, this measurement was carried out 2 times in each MOSFET. Then, we averaged the results to determine Ls.
Table II. The list of measured wiring parameter

<table>
<thead>
<tr>
<th>S1</th>
<th>Lg’ [nH]</th>
<th>Ld’ [nH]</th>
<th>Ls [nH]</th>
<th>Rs [Ω]</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>7.97</td>
<td>25.99</td>
<td>2.38</td>
<td>1.06</td>
</tr>
<tr>
<td>B</td>
<td>3.66</td>
<td>26.70</td>
<td>4.67</td>
<td>0.925</td>
</tr>
<tr>
<td>C</td>
<td>4.36</td>
<td>46.30</td>
<td>5.46</td>
<td>1.46</td>
</tr>
<tr>
<td>D</td>
<td>5.40</td>
<td>29.04</td>
<td>1.17</td>
<td>0.71</td>
</tr>
</tbody>
</table>

Next, according to the method of literature [17], the parasitic inductance \( L_g \) and \( L_d \) were measured by impedance analyzer (IM7581 Hioki E.E. Corp.) using the parallel LC resonant between parasitic inductance and capacitor of known capacity. In addition, parasitic resistor \( R_d \) was also measured using an impedance analyzer. In each measurement, we prepared another PCB with the same pattern as the experimental circuit similarly to the measurement of \( L_g \).

Firstly, the measurement circuit diagram of \( L_g \) is shown in Fig. 1(b). A small ceramic capacitor \( C_{mes1} \) was mounted on the pads for gate and source terminal of \( S_1 \). In addition, we made a solder bridge between the pad for driver output and ground terminal. Finally, both ends of \( C_{mes1} \) connected impedance analyzer. As a result, a parallel-connected LC resonator was composed of parasitic inductance \( L_g + L_s \) and the ceramic capacitor \( C_{mes1} \) in the gate current loop wiring path.

Then, we measured the frequency dependency of capacitor \( C_{mes1} \). When the resonant frequency at the peak impedance is defined as \( f_{rs} \), \( L_g' \) can be obtained as

\[
L_g' = \frac{1}{4\pi^2 f_{rs}^2 C_{mes1}} - L_s.
\]

Next, the measurement circuit diagram of \( L_d \) is shown in Fig. 1(c). We mounted a small ceramic capacitor \( C_{mes2} \) on the pads for drain and source terminals. Also, we made a solder bridge the pads for both ends of \( C_{mes2} \). In addition, we made a solder bridge between anode and cathode terminal of high-side parasitic diode. Moreover, to consider the parasitic inductance included in the current probe, a current probe inserted. Finally, both ends of \( C_{mes2} \) connected impedance analyzer. As a result, a parallel-connected LC resonator was composed of parasitic inductance \( L_d + L_s \) and the ceramic capacitor \( C_{mes2} \) in drain current loop wiring path.

Then, we measured the frequency dependency of capacitor \( C_{mes2} \). When the resonant frequency at the peak impedance is defined as \( f_{ds} \), \( L_d' \) can be obtained as

\[
L_d' = \frac{1}{4\pi^2 f_{ds}^2 C_{mes2}} - L_s.
\]

At last, the measurement of \( R_s \) was taken with the circuit from which \( C_{mes2} \) was removed in Fig. 1(c), and measured the frequency dependency of the resistance component. We determined the resistance value at resonant frequency \( f_{ds} \) as \( R_d \). The measurement results are shown in Table II.

B. Modeling of device

In this subsection, we model the switching device so that the characteristics can fit the measurement data. In order to achieve this purpose, we used the device model provided by the manufacturer and the characteristics were adjusted to its measurement data.

The experimental value of parasitic capacitance and \( I_{ds}-V_{gs} \) characteristics were measured by curve tracers CS-3300 and CS-605 (IWATSU ELECTRIC CO., LTD.), respectively. Parasitic capacitance was measured for \( V_{ds} \) of 0 to 100V and frequency of 1MHz. Also, \( I_{ds}-V_{gs} \) characteristics were measured for \( I_{ds} \) of 0 to approximately 10A. These measurements were performed on three different elements of the same model number. We averaged the acquired values and this was made into the measurement value.

Here, we modeled the device in PSPice. First, the parasitic capacitance included in the device model adjusted to be as negligible as possible. \( C_s \) and \( C_{gs} \) with the dependence of \( V_{ds} \) were modeled using external voltage-controlled current sources GVALUE. The product of the capacity table and the time derivative of \( V_{ds} \) is described for these current sources. \( C_{gs} \)
without the dependency of $V_{ds}$ was modeled by an ideal capacitor except for the remaining capacity in the device model.

Next, we focused on the fact that the $I_d$ can be changed by the ratio of the channel width $W$ to the channel length $L$, these parameters in the device models were adjusted. The modeling result is shown in Fig. 2. Manufacturer model is a device model provided by the manufacturer, and the tuning model is a device model that was tuned according to the method in this subsection. As shown in the Fig.2, we were able to model more accurate than the device model provided by the manufacturer.

Also, Fig. 3 shows the configured MOSFET model in PSpice. Moreover, Fig.4(a) shows the modeling circuit diagram of $C_{gd}$ in the conventional model. In addition, to avoid convergence errors, we inserted a 100mΩ resistor in series with $C_{gd}$ that does not affect the waveform.

### III. PROPOSED MODEL

The proposed model added the dependence of $V_{gs}$ on $C_{gd}$ from the conventional model and described two variables function of $V_{ds}$ and $V_{gs}$. Also, to extract its characteristics, two kinds of measurement circuits shown in Fig. 5 were used.

The first measurement circuit diagram is shown in Fig. 5(a). To make high-frequency pulsation voltage, DC voltage $V_{ds}$ supplied by DC voltage source and AC voltage $v_{ds}$ outputted by a signal generator. Next, to observe the AC voltage, the ceramic capacitor $C_1$ for cutting the DC voltage is connected in series with the resistor $R_1$ and $R_x$.

Also, Fig.5(a) is based on the idea of the bridge circuit. In the AC equivalent circuit, the bridge circuit is composed of $R_1$, $R_x$, $C_{gd}$, and $C_{gs}$ because $C_1$ is short and $R_2$ is much higher impedance than $C_{gs}$. In addition, to investigate the dependence of $V_{gs}$, the DC voltage source is connected between the gate and source of MOSFET. In order for this bridge circuit to satisfy the equilibrium condition, the voltage drop of $v_x$ and $v_{gs}$ must be equal. At this time, the amplitude of $v_x$ and $v_{gs}$ is the same. To satisfy this condition, the variable resistance $R_x$ is adjusted. Finally, we apply the balance condition in this circuit, $C_{gd}$ is obtained as

$$C_{gd} = \frac{R_x}{R_1} C_{gs}.$$  \hspace{1cm} (4)

In this paper, this measurement was carried out for DC voltage $V_{ds}$ of 0 to 100V, $V_{gs}$ of 0 to about 3V before the MOSFET turns on and frequency of 1MHz.

Next, another measurement circuit diagram is shown in Fig.5(b). We applied a high-frequency voltage from the impedance analyzer and measured capacitance component. Furthermore, the high impedance resistance 1MΩ is open and
TABLE III. EXTRACTED PARAMETERS OF APPROXIMATE EXPRESSION

<table>
<thead>
<tr>
<th>Param</th>
<th>Device (S1)</th>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>1640 × 10^9</td>
<td>1300 × 10^9</td>
<td>960 × 10^9</td>
<td>1057.7 × 10^9</td>
</tr>
<tr>
<td>B1</td>
<td>0.066</td>
<td>0.782</td>
<td>6.4823</td>
<td>0.9961</td>
<td></td>
</tr>
<tr>
<td>B2</td>
<td>1.15</td>
<td>2.072</td>
<td>0.001</td>
<td>0.631</td>
<td></td>
</tr>
<tr>
<td>C</td>
<td>0.0001</td>
<td>0.0666</td>
<td>0.0927</td>
<td>0.0504</td>
<td></td>
</tr>
<tr>
<td>D1</td>
<td>784.7 × 10^9</td>
<td>850.29 × 10^9</td>
<td>549 × 10^9</td>
<td>103.103 × 10^9</td>
<td></td>
</tr>
<tr>
<td>D2</td>
<td>0</td>
<td>30.88</td>
<td>1.2069</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>E</td>
<td>0.26</td>
<td>0.465</td>
<td>0.8824</td>
<td>0.2166</td>
<td></td>
</tr>
<tr>
<td>Cbias</td>
<td>25 × 10^9</td>
<td>20 × 10^9</td>
<td>4345 × 10^9</td>
<td>1.5 × 10^9</td>
<td></td>
</tr>
</tbody>
</table>

Ceramic capacitors 1µF are short in the AC circuit because these have a sufficiently larger capacity than parasitic capacitor of MOSFET. Therefore, the following composite capacitance C' can be measured

\[ C' = C_{gs} + \frac{C_{gd}C_{gs}}{C_{gs} + C_{gd}}. \]  (5)

Here, the measured value of the curve tracer at the same Vds in section II was adopted as the value of Cgs. Therefore, when the ratio Rg/R1 is k, Cgs is obtained as follows from (4) and (5):

\[ C_{gs} = \frac{-(1 + k)C_{ds} - kC_{ds}}{2kC_{ds}}. \]  (6)

Figure 6 shows the measurement results of Cgd. As shown in Fig.6, Cgd tended to increase as Vgs increased. In addition, there was a tendency that the smaller Vds, the stronger dependence of Cgd on Vgs. Next, to do modeling in PSpice, we carried out a curve fitting from the measurement result using approximate equations. Similar to section II, an external voltage-controlled current source was used in Cgd and analog behavior model ABM2/I was used so that we can use the two variables function. Figure 4(b) is the modeling circuit of Cgd in the proposed model. This circuit is composed of the editable part and offsets part Cbias. The editable part expresses the dependence of vgs and vgs. Also, the editable part composed of two kinds of the capacitor, Cg is used the function of vds, Cb has used the function of vgs. By connecting these in series, it is possible to describe a two-variable function. When the parameters to be fitted are from A to E, Cg and Cb are expressed by the following approximate expressions:

\[ C_g(v_{ds}) = \frac{A}{(B_1 + B_2v_{gs} + B_3v_{gs}^2)} e^{-C_{bias}}. \]  (7)

\[ C_b(v_{gs}) = (D_1 + D_2v_{gs}) e^{B_{bias}}. \]  (8)

In this paper, we fitted by the solver and each parameter was extracted. This fitting carried out the device in Table I and the extracted parameters are shown in Table III. The modeling circuit of MOSFET is Fig.3 and is the same as the conventional model. The circuit diagram of Cgd is changed to Fig.4(b). Cg and Cb are collectively expressed using the voltage-controlled current sources ABM2/I with two inputs.

IV. SWITCHING WAVEFORM COMPARISON

In this section, switching waveform is compared with conventional, proposed model and experimental results to evaluate the prediction accuracy of these models. To compare the switching waveforms, we measured by DPT with each S1.

A. Modeling circuit

Figure 7 shows the modeling circuit of DPT in PSpice. This circuit had a half-bridge structure and was used the same model number MOSFET S1. Next, S1 on high-side shorted between the gate and source terminal and the inductor was connected in parallel. C1 which the high-frequency current flows dominantly and S1 used the device model of the same model number provided by the manufacturer. Also, we used Si8261BAC (Silicon Laboratories Inc.) as gate driver and output impedance of gate driver Rgd has adopted the value in the datasheet [18]. It was 0.8Ω at turn-off and 2.6Ω at turn-on, respectively. Moreover, to reproduce the behavior of gate driver in PCB, the rise and fall times of the pulse voltage applied between the gate and source of low side’s S1 adopted the value of datasheet [18], and were 4.3ns, 9.7ns, respectively.
B. Results

Figure 8 shows a photograph of the experimental circuit at TO-220 packages. In this experiment, we supplied the circuit with \(E_1\) of 40V and drain current 10A. However, in the Device C, oscillatory false triggering [17] occurred, so we inserted a small-sized ceramic capacitor between the drain and the gate terminal of it and a U-shaped wire in the experimental PCB, and measured at 20V, 3A. Furthermore, the gate voltage of \(S_1\) was set at 10V and applied only two pulse. The first pulse width was determined based on the drain current we wanted to apply to \(S_1\) and we observed turn-off waveform when the first pulse falls. Besides, we observed the turn-on waveform when the second pulse rises.

The list and frequency band of experimental instruments is shown in Table IV. We confirmed that the resonant frequency in the switching waveform didn’t exceed the frequency band when we measured the switching waveform.

First, the switching waveforms at \(R_g\) of 150Ω and 10Ω for device D, which especially improved the prediction accuracy, are shown in Fig.9 and Fig.10, respectively. The deviations that occurred at the rise of the \(v_{ds}\) waveform and the mirror period of \(v_{gs}\) waveform in turn-off were improved, and the \(i_d\) waveform was almost the same. Therefore, it is considered that the prediction accuracy of turn-off loss is improved. On the other hand, turn-on waveforms didn’t almost change. This is thought to be because \(C_{gd}\) at turn-on was a smaller contribution to switching waveform than a turn-off. Also, there is a difference in the overshoot of the \(i_d\) at turn-on. This difference was attributed to the reverse recovery characteristics of the anti-parallel diode on the high-side, which was not considered in this

<table>
<thead>
<tr>
<th>Instrument</th>
<th>Part Number (Manufacturer)</th>
<th>Frequency band</th>
</tr>
</thead>
<tbody>
<tr>
<td>Oscilloscope</td>
<td>HD04034A (Teledyne Lecroy)</td>
<td>350MHz</td>
</tr>
<tr>
<td>Passive probe</td>
<td>PP021 (Teledyne Lecroy)</td>
<td>500MHz</td>
</tr>
<tr>
<td>Current probe</td>
<td>TCP312 (Tektronix)</td>
<td>100MHz</td>
</tr>
</tbody>
</table>

Fig.9. Switching waveform at 40V, 10A, \(R_g\) 150Ω, and Device D.

Fig.10. Switching waveform at 40V, 10A, \(R_g\) 10Ω, and Device D.

Fig.11. Comparison of \(v_{ds}\) waveforms in other devices at \(R_g\) 150Ω

Fig.12. Comparison of turn-off loss of 40V, 10A and Device D

<table>
<thead>
<tr>
<th>Gate resistance [Ω]</th>
<th>Turn-off energy loss [μJ]</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.3</td>
<td>0.6</td>
</tr>
<tr>
<td>10</td>
<td>0.8</td>
</tr>
<tr>
<td>33</td>
<td>1.0</td>
</tr>
<tr>
<td>68</td>
<td>1.2</td>
</tr>
<tr>
<td>100</td>
<td>1.4</td>
</tr>
<tr>
<td>150</td>
<td>1.6</td>
</tr>
</tbody>
</table>
model. However, $i_d$ waveform at turn-on from 0 to 10A with adjusted $I_{DSw}$ characteristics shows a good prediction.

Next, Fig.11 shows the $v_{ds}$ waveform at the turn-off of other devices. Device A was almost the same waveform. On the other hand, in device B and C, the slope of the $v_{ds}$ waveform approached the experiment.

Finally, Fig.12 shows the result of comparing the turn-off loss of device D at 40V, 10A. The turn-off loss ranged from the point where $v_{ds}$ rises to 10% of set value to the point where $i_d$ falls to 10% of set value and turn-off loss was dominant in this range. From this figure, similar to the turn-off waveform, it was confirmed that the consideration of the $C_{gd}$ on $v_{gs}$ had a tendency to reduce the deviation from the experiment compared to the no consideration it. From the above, it was revealed that the consideration of the $C_{gd}$ on $v_{gs}$ has the ability to improve the prediction accuracy of the switching waveforms.

V. CONCLUSION

Predicting the switching waveforms is indispensable for future miniaturization and higher density of power conversion circuits. In this paper, we verified the improvement of prediction accuracy by whether or not considering the dependence of the gate-drain capacitance on gate-source voltage. To construct the modeling circuit, we measured wiring parameter and characteristic of the MOSFET. As a result of comparing the switching waveforms, the model considered the dependence of the gate-drain capacitance on gate-source voltage showed that the prediction accuracy of turn-off waveforms tended to improve at the rise of the drain-source voltage and at the fall of the gate-source voltage. Therefore, it was revealed that this consideration has the ability to predict the accuracy of the turn-off waveforms and the turn-off loss.

REFERENCES


